



Bare Die

SiC Power MOSFETs

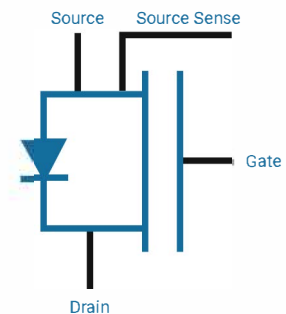
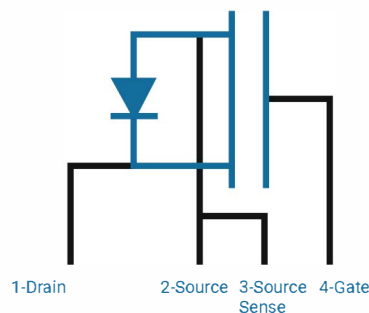
Cactus Material MOSFETs exceed power, efficiency and portability capabilities of standard silicon devices and are available in a variety of breakdown voltages (650V, 1200V, 1700V & 3300V) and current ratings. They have low on-resistance and low leakage in the blocking state. Fabricated on high-quality SiC epitaxial layers, our proprietary fabrication process includes carefully chosen annealing procedures to ensure a high-quality SiC-SiO₂ gate oxide dielectric layer. Doping profile, neck region, and edge termination ensure extremely low Ron and high breakdown voltage.

BENEFITS

- ✓ Higher efficiency
- ✓ Reduced cooling
- ✓ Increased power
- ✓ Reduced system volume

APPLICATIONS INCLUDE

Electromechanical power converters, DC to DC, AC to DC and DC to AC converters, switching power supplies, electric vehicles, hybrid vehicles, solar and wind energy power converters.



Part Number	Package	Marking
C080SCM33070A	Bare Die	Cactus Materials

Gen-II MOSFET with body diode | 40A - 3300V SiC MOSFET

Maximum Ratings						
*Characteristics	Symbol	Comments	Min	Typ	Max	Units
DC blocking voltage	V_{DSmax}	$T_J=25^\circ\text{C}$ to 175°C	3300			V
Gate input voltage range	V_{GS}	Recommended range Dynamic	-5 -7		20 23	V
Avalanche rating	V_{AVA}	$V_{GS}=0\text{V}; I_{DS}=100\mu\text{A}; T_J=25^\circ\text{C}$ $V_{GS}=0\text{V}; I_{DS}=100\mu\text{A}; T_J=175^\circ\text{C}$	3300	>4300		
Pulsed drain current	$I_{Dpulsed}$	$V_{GS}=20\text{V}; T_J=25^\circ\text{C}$ $V_{GS}=20\text{V}; T_J=100^\circ\text{C}$ limited by $T_J, t_p=300\mu\text{s}$		100 70		A
Continuous drain current	I_D	$V_{GS}=20\text{V}; T_J=25^\circ\text{C}$ $V_{GS}=20\text{V}; T_J=100^\circ\text{C}$			40 30	A
Continuous drain power	P	$V_{GS}=20\text{V}; T_J=25^\circ\text{C}$			210	W
Maximum-junction temperature	T_{jmax}	Normal operation During processing/soldering			195 250	$^\circ\text{C}$

Electrical and Thermal Characteristics						
*Characteristics	Symbol	Comments	Min	Typ	Max	Units
Gate threshold voltage	V_{TH}	$V_{DS}=1\text{V}; I_{DS}=20\text{mA}; T_J=25^\circ\text{C}$ $V_{DS}=1\text{V}; I_{DS}=20\text{mA}; T_J=175^\circ\text{C}$	2.78	2.88 1.64	2.98	V
Gate leakage	I_{GSS}	$V_{GS}=20\text{V}; V_{DS}=0; T_J=25^\circ\text{C}$ $V_{GS}=20\text{V}; V_{DS}=0; T_J=175^\circ\text{C}$		5 150		pA
Drain leakage	I_{DSS}	$V_{DS}=1000\text{V}; V_{GS}=0; T_J=25^\circ\text{C}$ $V_{DS}=1000\text{V}; V_{GS}=0; T_J=175^\circ\text{C}$		0.05 50		nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=20\text{V}; I_{DS}=30\text{A}; T_J=25^\circ\text{C}$ $V_{GS}=20\text{V}; I_{DS}=30\text{A}; T_J=175^\circ\text{C}$ $V_{GS}=20\text{V}; I_{DS}=40\text{A}; T_J=25^\circ\text{C}$ $V_{GS}=20\text{V}; I_{DS}=40\text{A}; T_J=175^\circ\text{C}$	65	70 315 75 325	75	m Ω
Transconductance	G_m	$V_{DS}=10\text{V}; I_{DS}=40\text{A}; T_J=25^\circ\text{C}$ $V_{DS}=10\text{V}; I_{DS}=30\text{A}; T_J=25^\circ\text{C}$ $V_{DS}=10\text{V}; I_{DS}=20\text{A}; T_J=175^\circ\text{C}$		13.8 12.5 7.5		S
Input capacitance	C_{ISS}			2750 / 2700		
Output capacitance	C_{OSS}	$V_{GS}=0\text{V}; V_{DS}=200 / 1000\text{V}$ $f=1\text{MHz}; T_J=25^\circ\text{C}$		182 / 67		pF
Reverse transfer capacitance	C_{RSS}			24.5 / 13.5		
Stored energy at output	E_{OSS}	Double integral of C_{OSS} (up to 1000V)		95		
Turn on switching energy (with body diode)	E_{ON}	$V_{GS}=-5/20\text{V}; V_{DD}=800\text{V}; R_{G(ext)}=0\Omega$ $I_{DS}=30\text{A}; L=80\mu\text{H}; T_J=25^\circ\text{C}$		960		μJ
Turn off switching energy (with body diode)	E_{OFF}	Clamped inductive switching waveform test circuit. Figure 26.		340		
Rise time	t_r	$V_{GS}=-5/20\text{V}; V_{DD}=800\text{V}; R_{G(ext)}=0\Omega$ $I_{DS}=30\text{A}; L=80\mu\text{H}; T_J=25^\circ\text{C}$		24		
Fall time	t_f	Clamped inductive switching waveform test circuit. Figure 26.		26		ns
Turn off delay time	$t_{d(on)}$ $t_{d(off)}$	Relative to V_{DS} inductive load. Figure 26.		50 80		
Gate Charge	Q_G	$V_{GS}=-5/20\text{V}; V_{DD}=800\text{V}; R_{G(ext)}=500\Omega$ $I_{DS}=17\text{A}; R_L=47\Omega; I_{GS}=45\text{mA}; T_J=25^\circ\text{C}$ Figure 27.		220		nC
Internal gate resistance	R_G	$f=1\text{Mz}; V_{AC}=25\text{mV}; T_J=25^\circ\text{C}$ Open drain		11		Ω
Thermal resistance: Junction to Case	R_{JC}			0.4		$^\circ\text{C/W}$

Body diode characteristics						
*Characteristics	Symbol	Comments	Min	Typ	Max	Units
Diode forward voltage	V_F	$I_F=5A; V_{GS}=0V; T_J=25^\circ C$ $I_F=5A; V_{GS}=0V; T_J=175^\circ C$ $I_F=10A; V_{GS}=-4V; T_J=25^\circ C$ $I_F=10A; V_{GS}=-4V; T_J=175^\circ C$		2.77 3.12 4.62 3.72		V
Pulsed diode current	$I_{S(pulsed)}$	$V_{GS}=0V; V_{DS}=-3V; T_J=25^\circ C$ $V_{GS}=0V; V_{DS}=-3V; T_J=175^\circ C$		6.9 4.56		A
Reverse recovery time	t_{rr}			30		ns
Reverse recovery charge	Q_{rr}	$V_{DD}=800V; V_{GS}=-4V; I_{DS}=20A$ $R_{G(ext)}=20\Omega L=180\mu H di/dt=1350A/\mu S$ Clamped inductive switching waveform test circuit: Figure 26		630		nC
Peak reverse recovery current	I_{RRM}			24		A

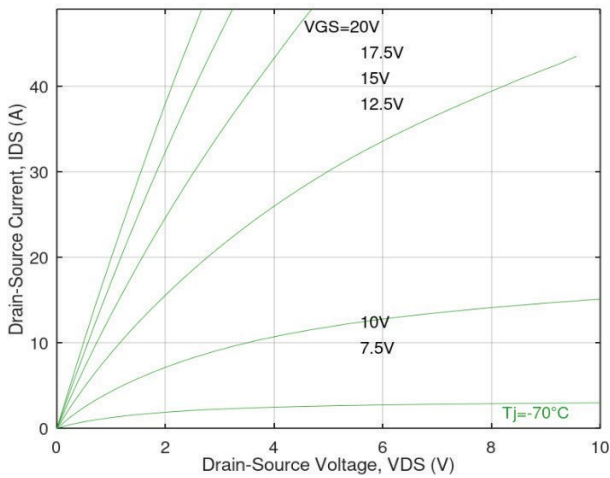


Figure 1: Low temperature output characteristics†.

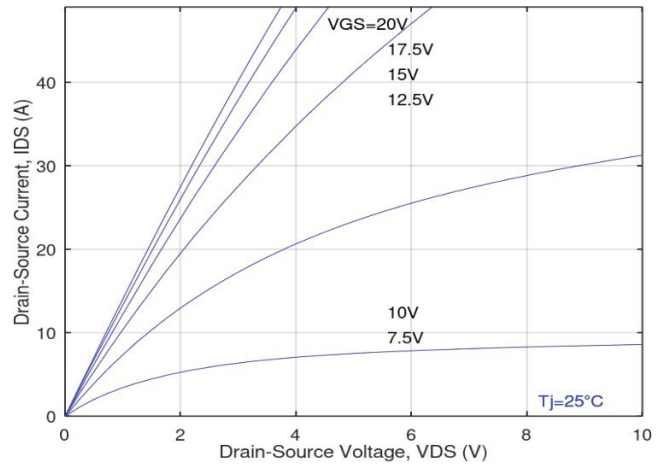


Figure 2: Room temperature output characteristics†.

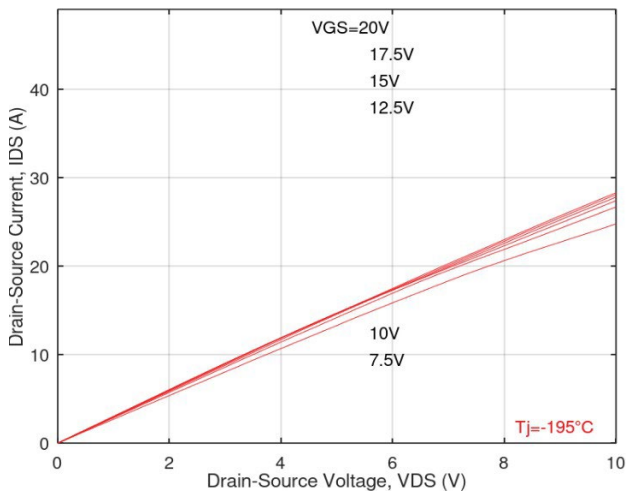


Figure 3: High temperature output characteristics†.

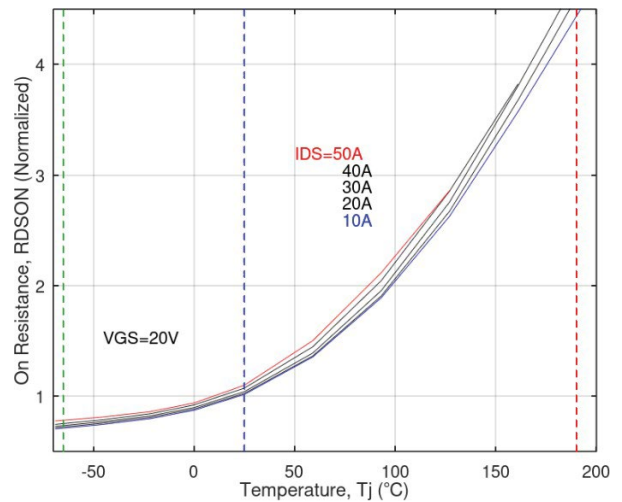


Figure 4: Normalized on-resistance vs. temperature. Dashed vertical lines indicate to room (25°C), high (190°C) and low (-65°C) temperatures.

† $t_p=300\mu s$ in pulsed IV measurements
 Unless stated otherwise, temperature corresponds to junction temperature.

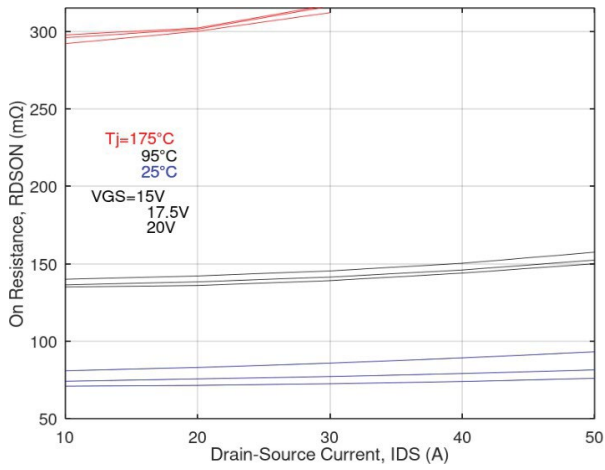


Figure 5: On-resistance vs. drain current.

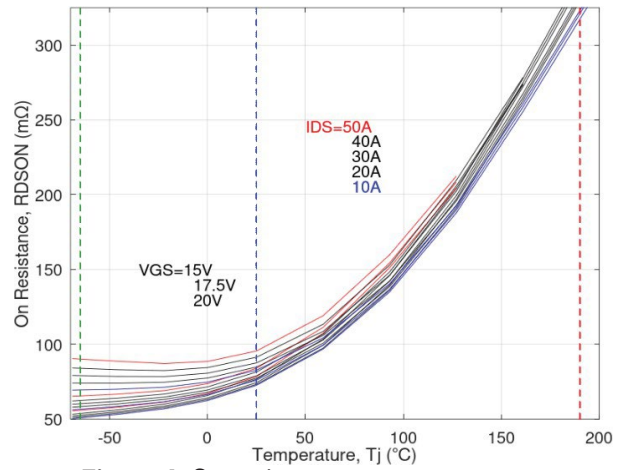


Figure 6: On-resistance vs. temperature. Dashed vertical lines indicate to room (25°C), high(190°C) and low (-65°C) temperatures.

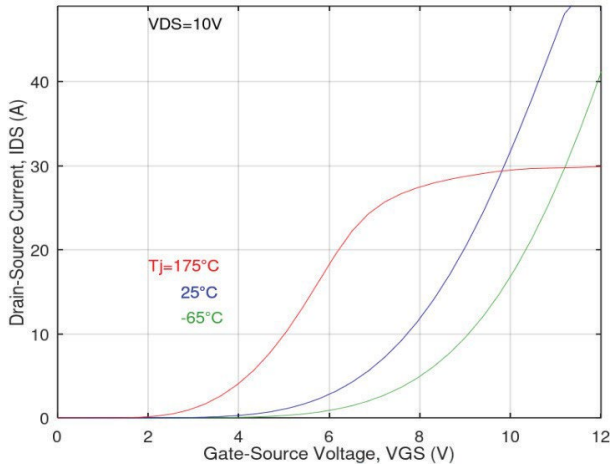


Figure 7: Transfer characteristics†.

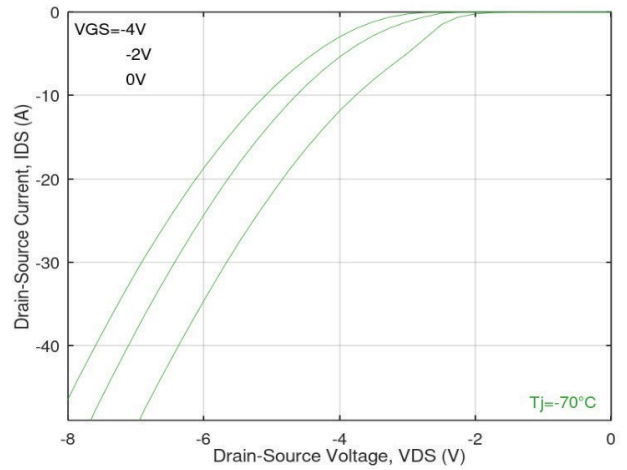


Figure 8: Low temperature body diode characteristics†.

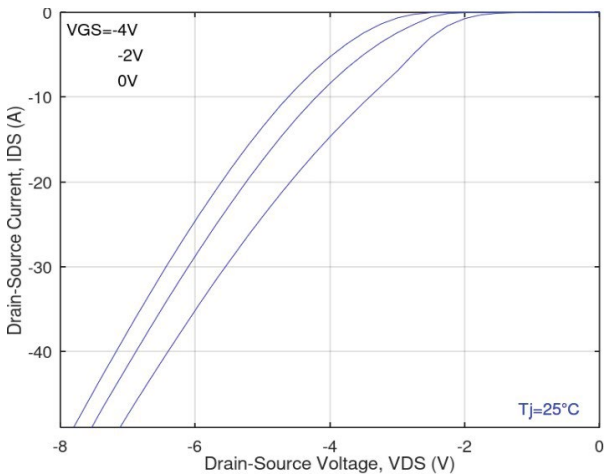


Figure 9: Room temperature body diode characteristics†.

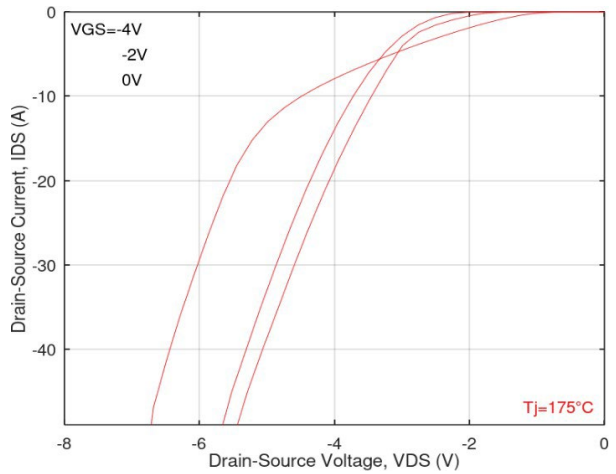


Figure 10: High temperature body diode characteristics†.

† $t_p=300\mu s$ in pulsed IV measurements
Unless stated otherwise, temperature corresponds to junction temperature.

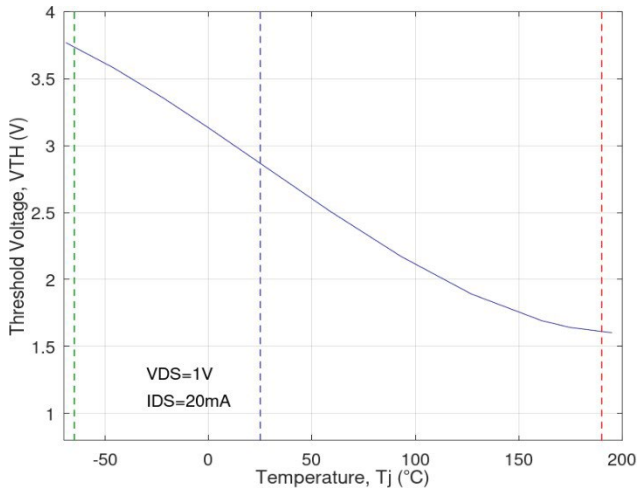


Figure 11: Threshold vs. temperature. Dashed vertical lines indicate to room (25 °C), high (190 °C) and low (-65 °C) temperatures.

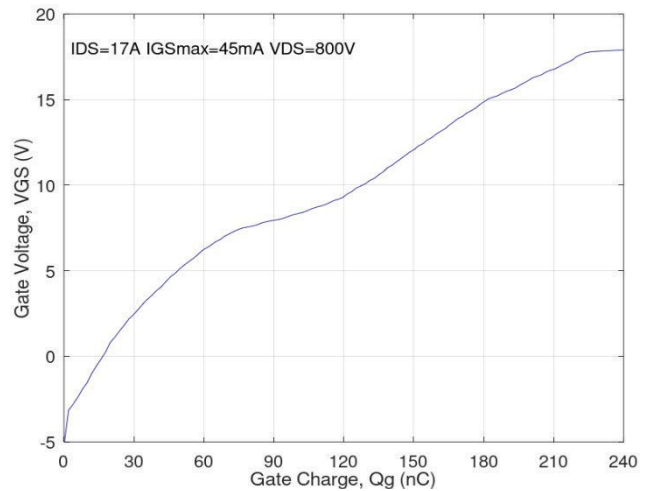


Figure 12: Gate charge characteristics

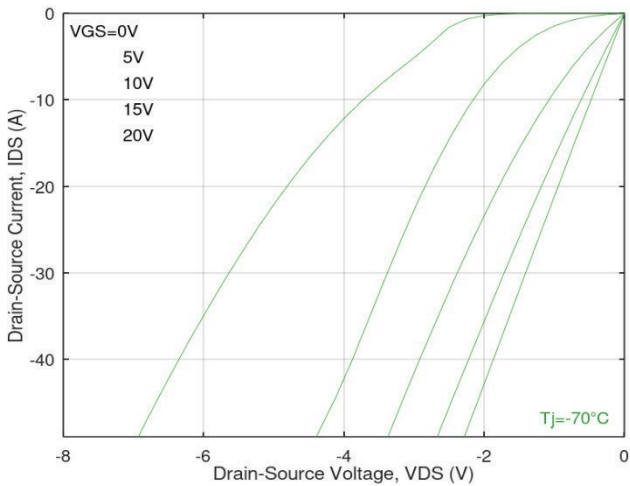


Figure 13: Low temperature third quadrant characteristics†.

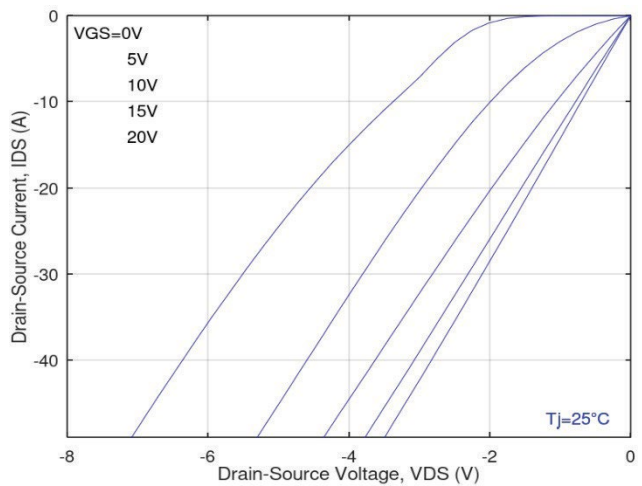


Figure 14: Room temperature third quadrant characteristics†.

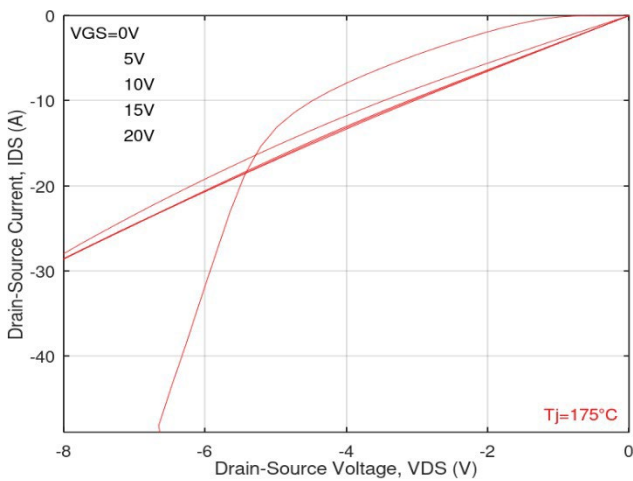


Figure 15: High temperature third quadrant characteristics†.

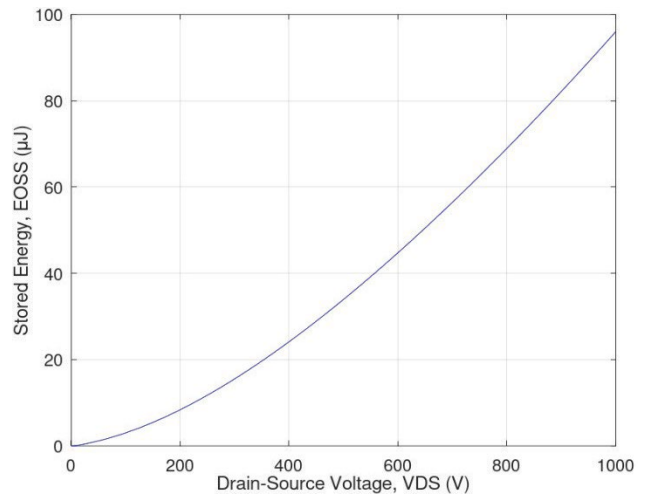


Figure 16: Output capacitor stored energy.

† $t_p=300\mu s$ in pulsed IV measurements
Unless stated otherwise, temperature corresponds to junction temperature.

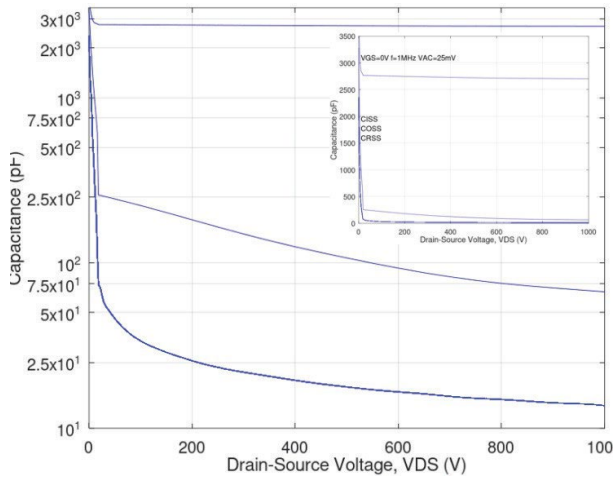


Figure 17: Capacitance vs. drain voltage.

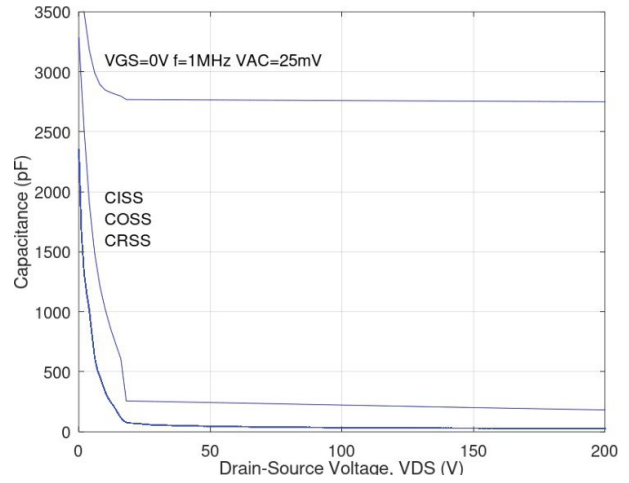


Figure 18: Capacitance vs. drain voltage.

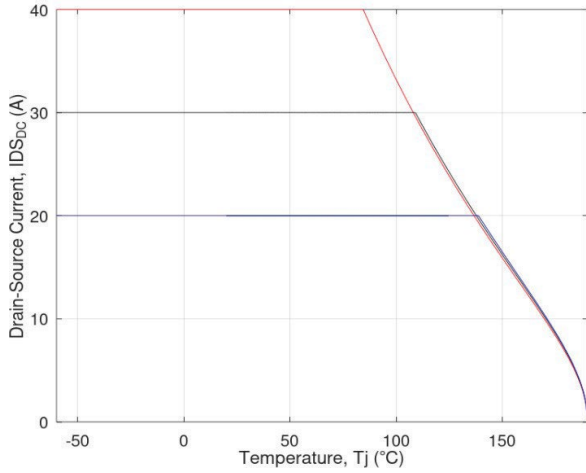


Figure 19: Continuous drain current vs. temperature.

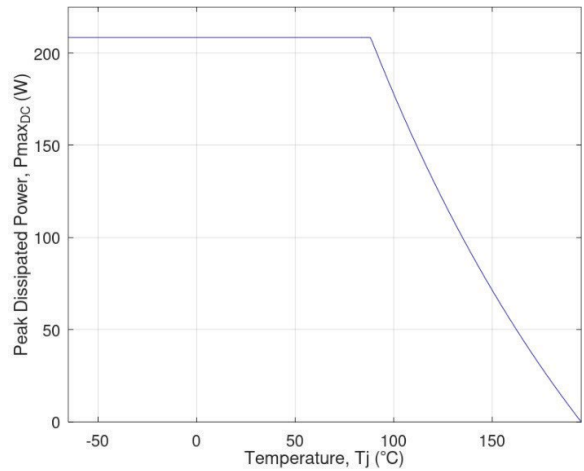


Figure 20: Power dissipation derating vs. temperature.

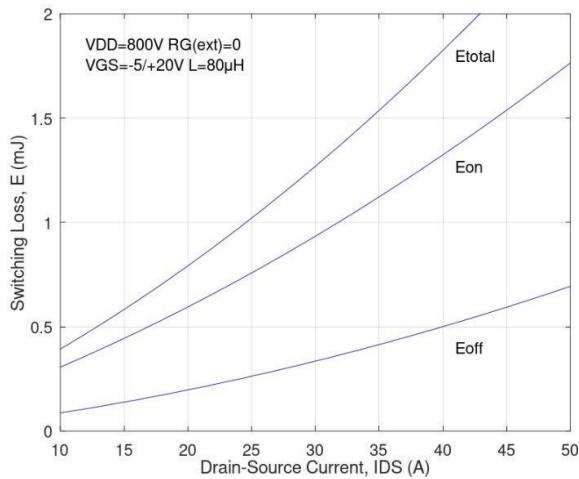


Figure 21: Clamped inductive switching energy vs. drain current at 800V VDD.

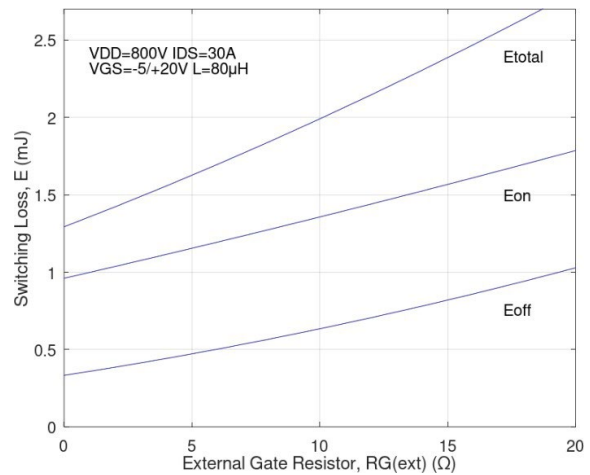


Figure 22: Clamped inductive switching energy vs. external gate resistance

Unless stated otherwise, temperature corresponds to junction temperature.

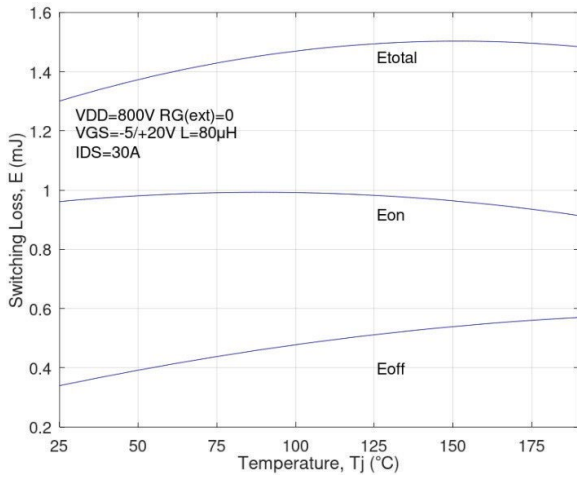


Figure 23: Clamped inductive switching energy vs. external gate resistance.

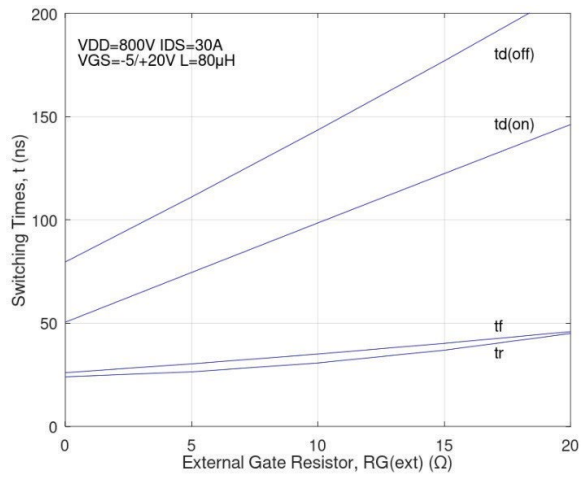


Figure 24: Clamped inductive switching energy vs. temperature.

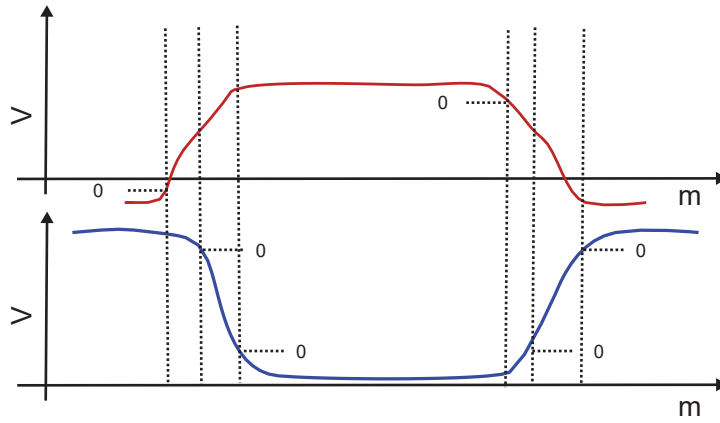


Figure 25: Timing references

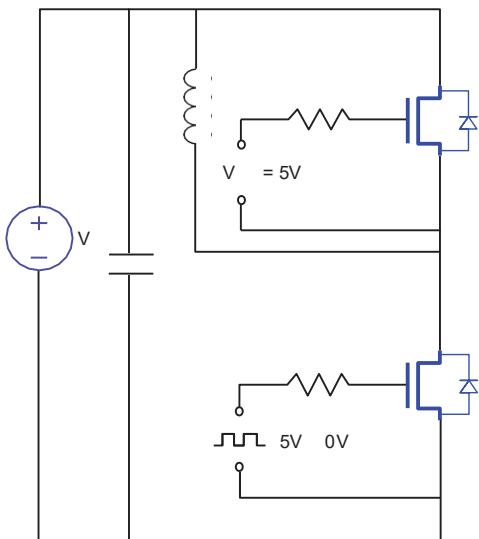


Figure 26: Clamped inductive switching waveform test circuit.

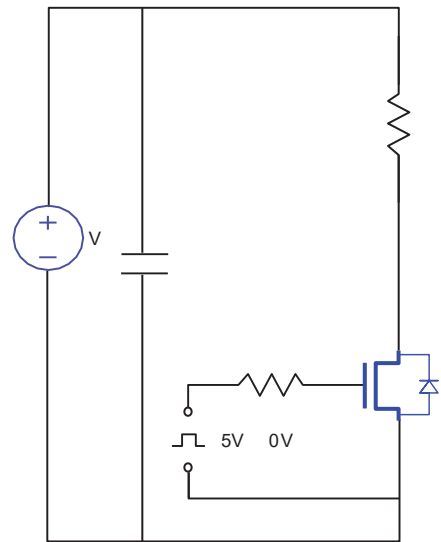


Figure 27: Gate charge test circuit.

Unless stated otherwise, temperature corresponds to junction temperature.

CAUTION: These devices are ESD sensitive. User proper handling procedures.

Disclaimer: The specifications provided are not a guarantee of component performance. It is essential to test components for their specific applications, as modifications may be required. Use of Cactus Materials components in life support systems and devices necessitates prior written approval from Cactus Materials.

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