Bare Die

SiC Power MOSFETs

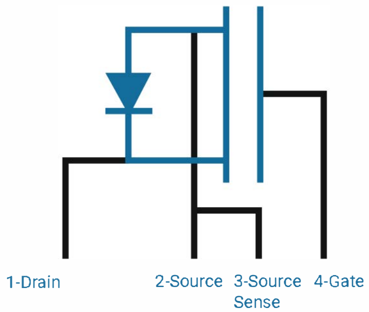
Cactus Material MOSFETs exceed power, efficiency and portability capabilities of standard silicon devices and are available in a variety of breakdown voltages (650V, 1200V, 1700V & 3300V) and current ratings. They have low on-resistance and low leakage in the blocking state. Fabricated on high-quality SiC epitaxial layers, our proprietary fabrication process includes carefully chosen annealing procedures to ensure a high-quality SiC-SiO2 gate oxide dielectric layer. Doping profile, neck region, and edge termination ensure extremely low
Ron and high breakdown voltage.

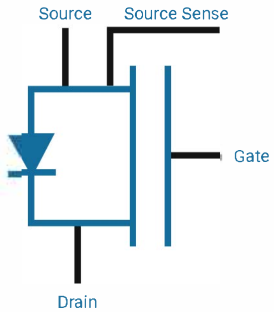
BENEFITS

- ☑ Higher efficiency
- ☑ Reduced cooling
- ☑ Increased power
- ☑ Reduced system volume

APPLICATIONS INCLUDE

Electromechanical power converters, DC to DC, AC to DC and DC to AC converters, switching power supplies, electric vehicles, hybrid vehicles, solar and wind energy power converters.





Part Number	Package	Marking
C080SCM33040A	Bare Die	Cactus Materials

Maximum Ratings

*Characteristics	Symbol	Comments	Min	Typ	Max	Units
DC blocking voltage	V_{DSmax}	T_J=25°C to 175°C	3300			V
Gate input voltage range	V_{GS}	Recommended range Dynamic	-5 -7		20 23	V
Avalanche rating	V_{AVA}	V_{GS}=0V; I_{DS}=100μA; T_J=25°C V_{GS}=0V; I_{DS}=100μA; T_J=175°C	3300	>4300		
Pulsed drain current	$I_{Dpulsed}$	V_{GS}=20V; T_J=25°C V_{GS}=20V; T_J=100°C limited by Tj, tp=300μS		100 70		A
Continuous drain current	I_D	V_{GS}=20V; T_J=25°C V_{GS}=20V; T_J=100°C			40 30	A
Continuous drain power	P	V_{GS}=20V; T_J=25°C			210	W
Maximum-junction temperature	T_{jmax}	Normal operation During processing/soldering			195 250	°C

Electrical and Thermal Characteristics

*Characteristics	Symbol	Comments	Min	Typ	Max	Units
Gate threshold voltage	V_{TH}	V_{DS}=1V; I_{DS}=20mA; T_J=25°C V_{DS}=1V; I_{DS}=20mA; T_J=175°C	2.78	2.88 1.64	2.98	V
Gate leakage	I_{GSS}	V_{GS}=20V; V_{DS}=0; T_J=25°C V_{GS}=20V; V_{DS}=0; T_J=175°C		5 150		pA
Drain leakage	I_{DSS}	V_{DS}=1000V; V_{GS}=0; T_J=25°C V_{DS}=1000V; V_{GS}=0; T_J=175°C		0.05 50		nA
Drain-source on-resistance	R_{DSON}	V_{GS}=20V; I_{DS}=30A; T_J=25°C V_{GS}=20V; I_{DS}=30A; T_J=175°C V_{GS}=20V; I_{DS}=40A; T_J=25°C V_{GS}=20V; I_{DS}=40A; T_J=175°C	65	70 315 75 325	75	mΩ
Transconductance	G_m	V_{DS}=10V; I_{DS}=40A; T_J=25°C V_{DS}=10V; I_{DS}=30A; T_J=25°C V_{DS}=10V; I_{DS}=20A; T_J=175°C		13.8 12.5 7.5		S
Input capacitance	C_{ISS}	V_{GS}=0V; V_{DS}=200 / 1000V f=1MHz; T_J=25°C		2750 / 2700		pF
Output capacitance	C_{OSS}			182 / 67		
Reverse transfer capacitance	C_{RSS}			24.5 / 13.5		
Stored energy at output	E_{OSS}	Double integral of C_{OSS}(up to 1000V)		95		μJ
Turn on switching energy (with body diode)	E_{ON}	V_{GS}–5/20V; V_{DD}=800V; $R_{G(ext)}$=0Ω I_{DS}=30A; L=80μH; T_J=25°C		960		
Turn off switching energy (with body diode)	E_{OFF}	Clamped inductive switching waveform test circuit. Figure 26.		340		
Rise time	t_r	V_{GS}=–5/20V; V_{DD}=800V; $R_{G(ext)}$=0Ω I_{DS}=30A; L=80μH; T_J=25°C Clamped inductive switching waveform test circuit. Figure 26. Relative to V_{DS} inductive load. Figure 26.		24		ns
Fall time	t_f			26		
Turn off delay time	$t_{d(on)}$ $t_{d(off)}$			50 80		
Gate Charge	Q_G	V_{GS}=–5/20V; V_{DD}=800V;$R_{G(ext)}$=500Ω I_{DS}=17A; R_L=47Ω; I_{GS}=45mA; T_J=25°C Figure 27.		220		nC
Internal gate resistance	R_G	f=1Mz; V_{AC}=25mV; T_J=25°C Open drain		11		Ω
Thermal resistance:Junction to Case	R_{JC}			0.4		°C/W

Body diode characteristics						
*Characteristics	Symbol	Comments	Min	Typ	Max	Units
Diode forward voltage	V_F	I_F=5A; V_{GS}=0V; T_J=25°C I_F=5A;V_{GS}=0V;T_J=175°C I_F=10A; V_{GS}=−4V; T_J=25°C I_F=10A; V_{GS}=−4V;T_J=175°C		2.77 3.12 4.62 3.72		V
Pulsed diode current	$I_{s(pulsed)}$	V_{GS}=0V; V_{DS}=-3V; T_J=25°C V_{GS}=0V; V_{DS}=-3V; T_J=175°C		6.9 4.56		A
Reverse recovery time	t_{rr}	V_{DD}=800V; V_{GS}=-4V; I_{DS}=20A $R_{G(ext)}$=20ΩL=180µH di/dt=1350A/µS Clamped inductive switching waveform test circuit: Figure 26		30		ns
Reverse recovery charge	Q_{rr}			630		nC
Peak reverse recovery current	I_{RRM}			24		A

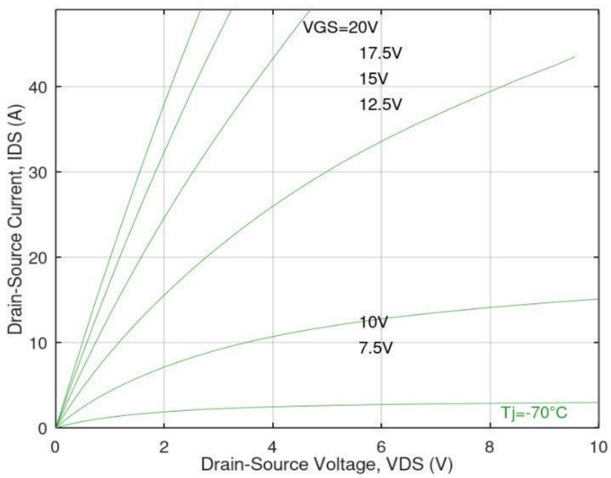


Figure 1: Low temperature output characteristics†.

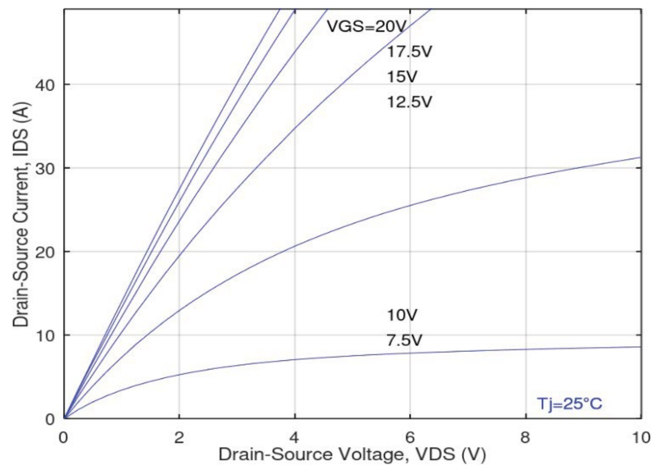


Figure 2: Room temperature output characteristics†.

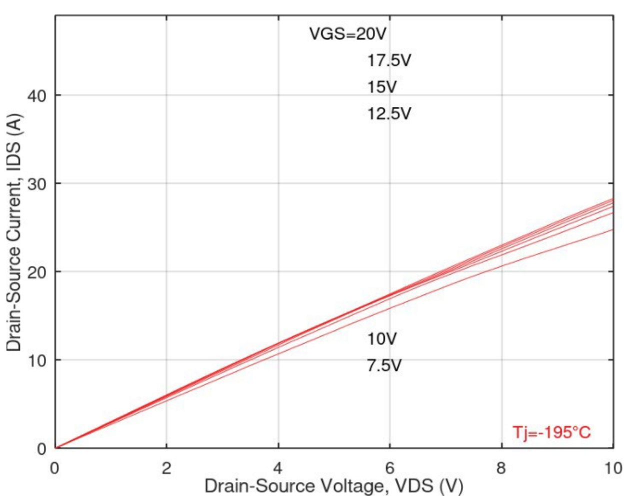


Figure 3: High temperature output characteristics†.

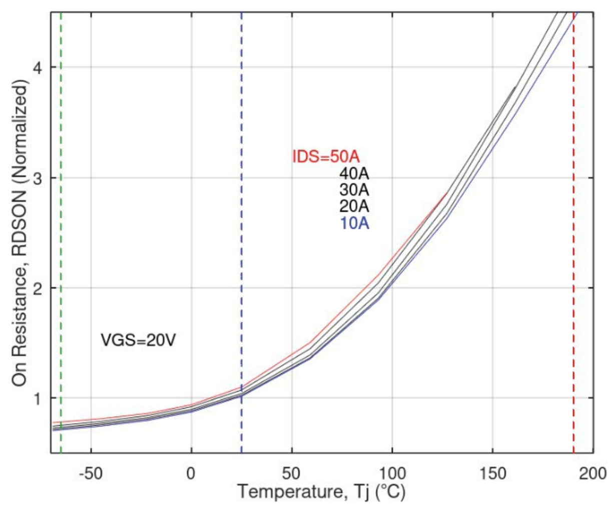


Figure 4: Normalized on-resistance vs. temperature. Dashed vertical lines indicate to room (25°C), high (190°C) and low (-65°C) temperatures.

† tp=300µs in pulsed IV measurements
Unless stated otherwise, temperature corresponds to junction temperature.

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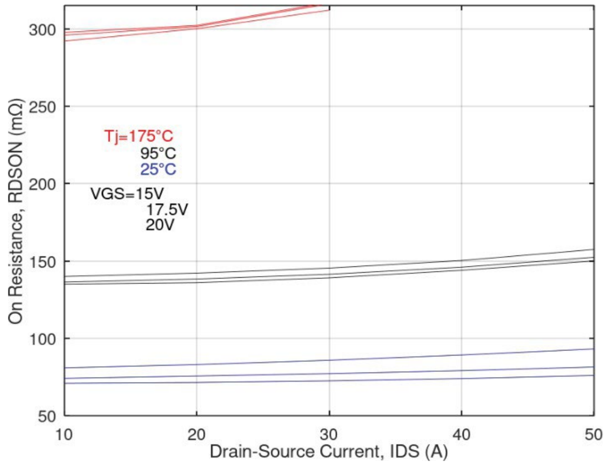

Figure 5: On-resistance vs. drain current.

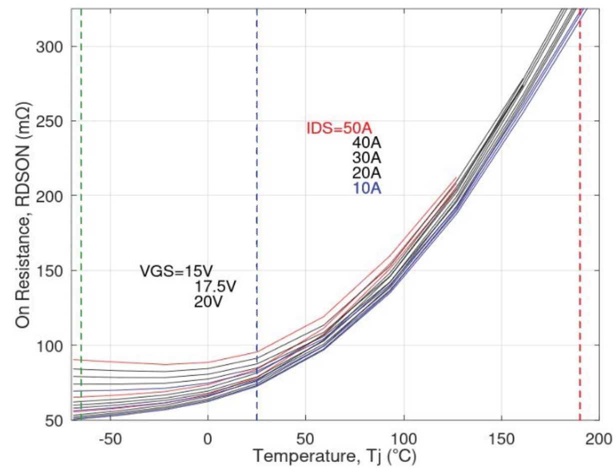

Figure 6: On-resistance vs. temperature. Dashed vertical lines indicate to room (25°C), high(190°C) and low (-65°C) temperatures.

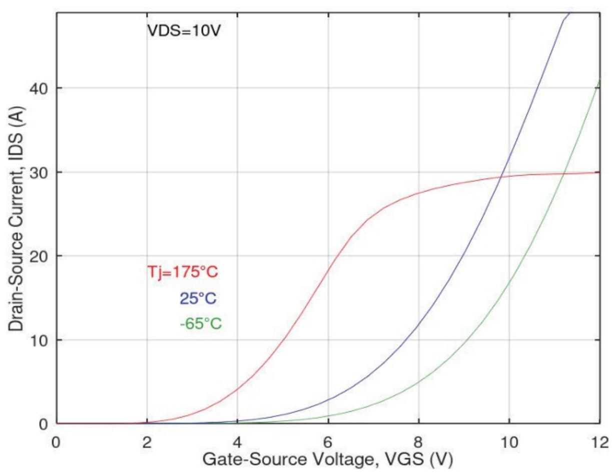

Figure 7: Transfer characteristics†.

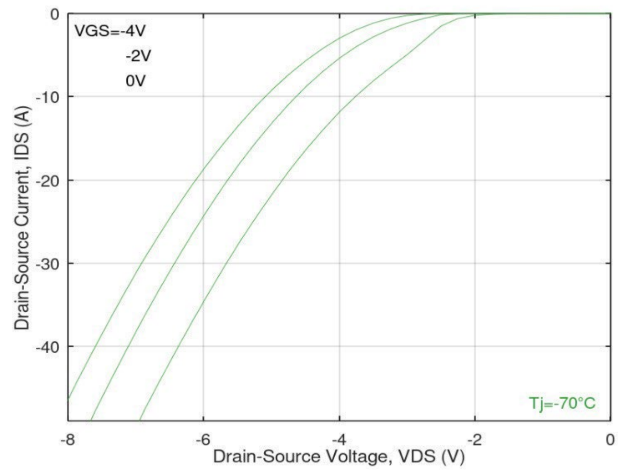

Figure 8: Low temperature body diode characteristics†.

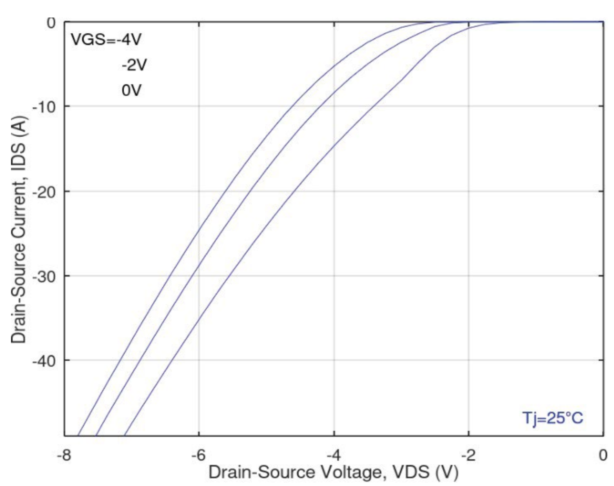

Figure 9: Room temperature body diode characteristics†.

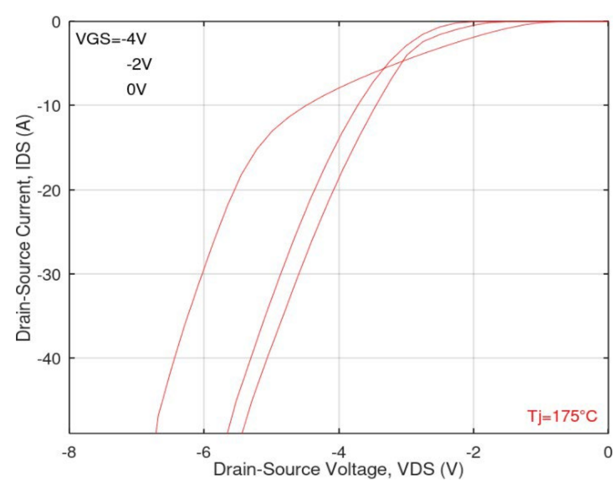

Figure 10: High temperature body diode characteristics†.

† tp=300μs in pulsed IV measurements
Unless stated otherwise, temperature corresponds to junction temperature.

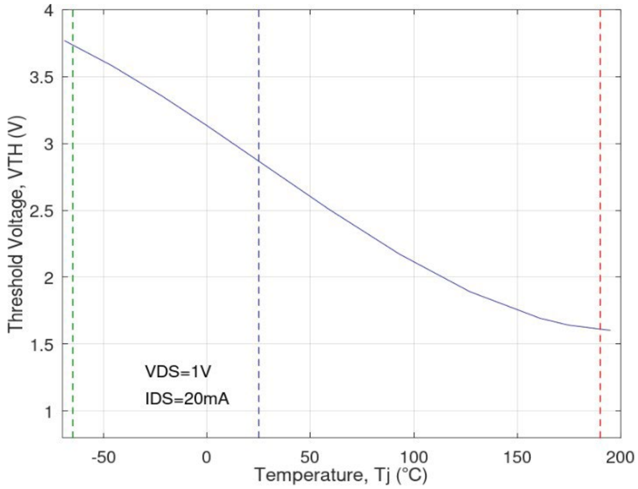

Figure 11: Threshold vs. temperature.
Dashed vertical lines indicate to room (25°C), high (190°C) and low (-65°C) temperatures.

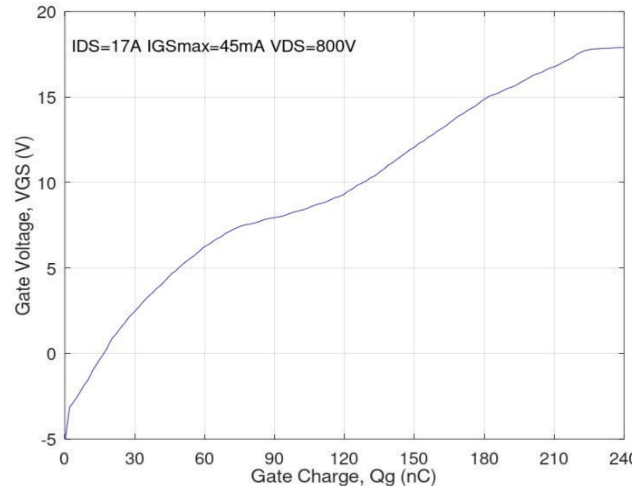

Figure 12: Gate charge characteristics

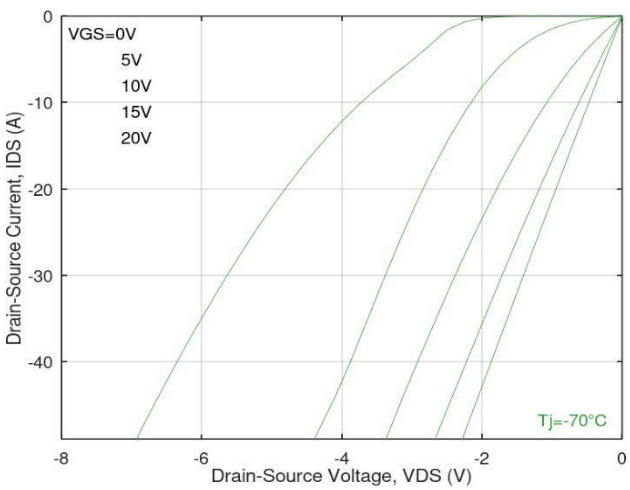

Figure 13: Low temperature third quadrant characteristics†.

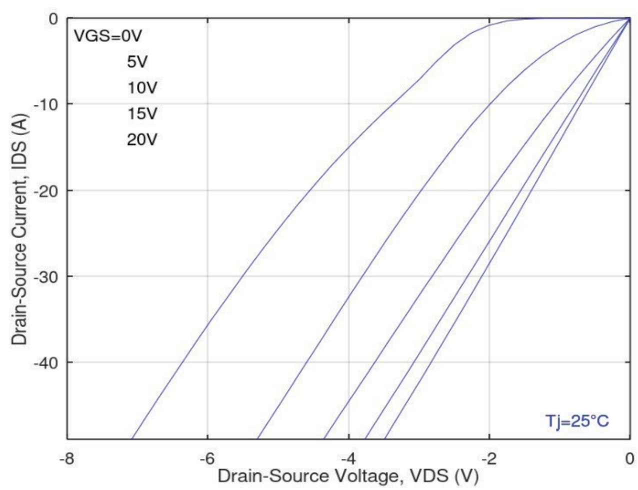

Figure 14: Room temperature third quadrant characteristics†.

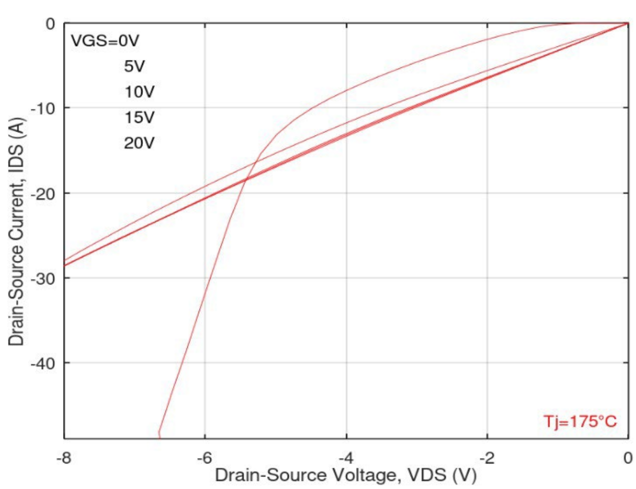

Figure 15: High temperature third quadrant characteristics†.

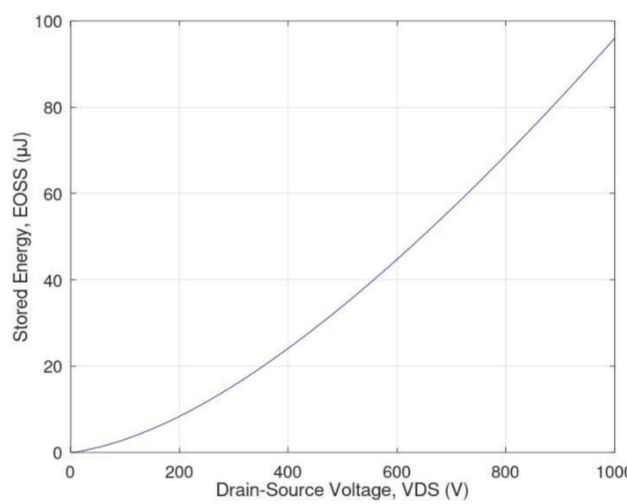

Figure 16: Output capacitor stored energy.

† tp=300μs in pulsed IV measurements
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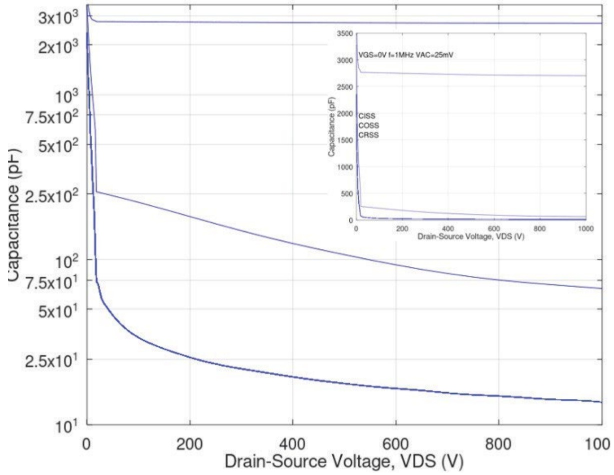

Figure 17: Capacitance vs. draing voltage.

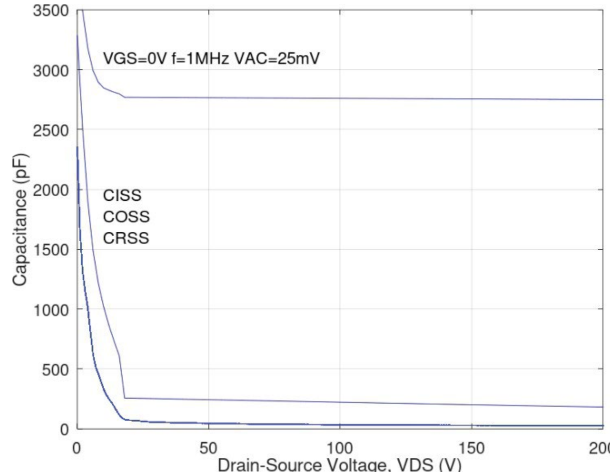

Figure 18: Capcitance vs. drain voltage.

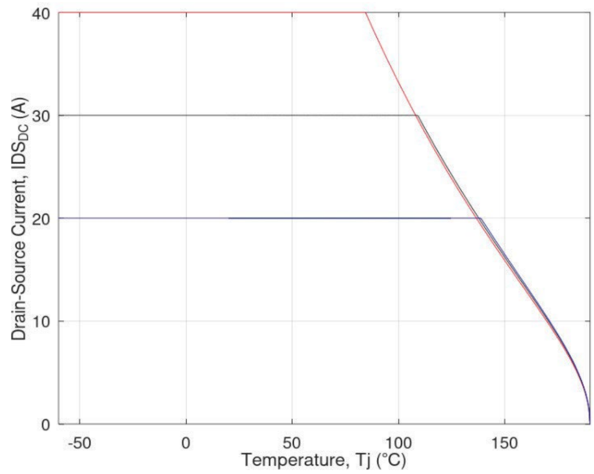

Figure 19: Continuous drain current vs. temperature.

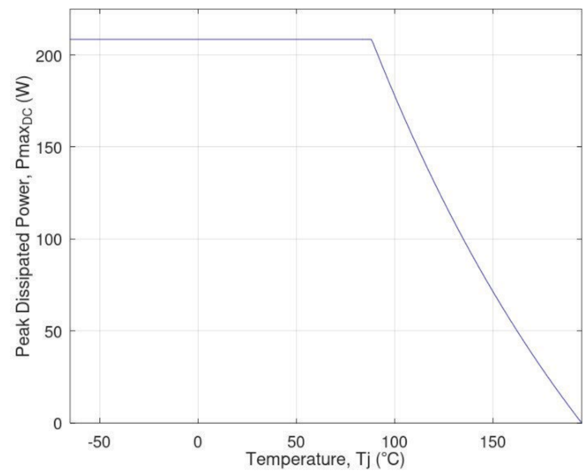

Figure 20: Power dissipation derating vs. temperature.

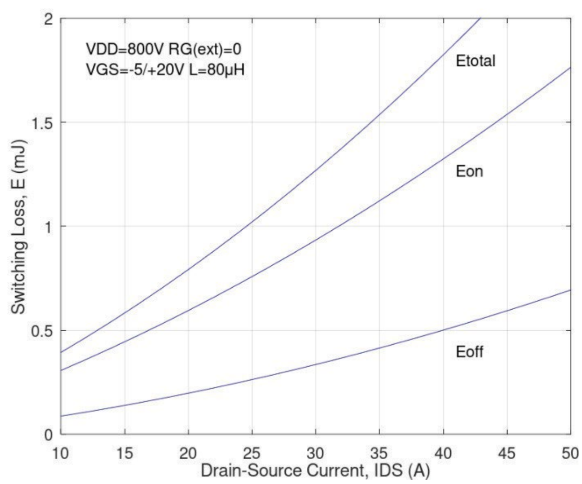

Figure 21: Clamped inductive switching energy vs. drain current at 800V VDD.

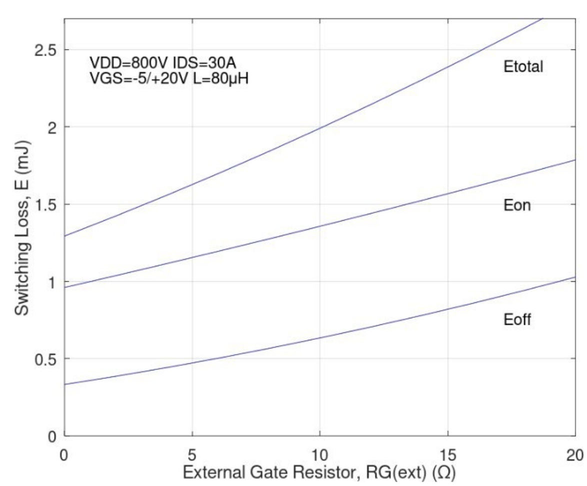

Figure 22: Clamped inductive switching energy vs. external gate resistance

Unless stated otherwise, temperature corresponds to junction temperature.

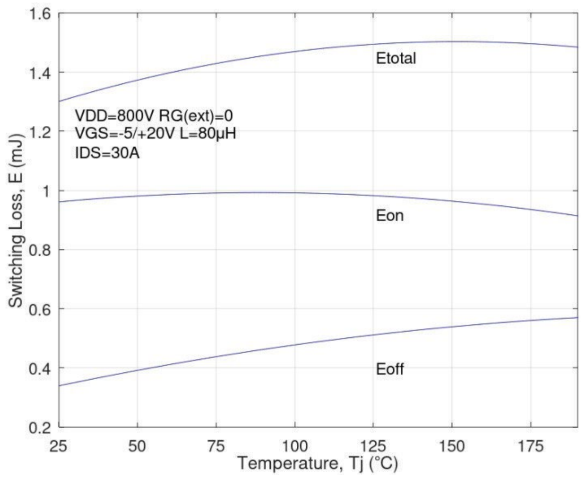

Figure 23: Clamped inductive switching energy vs. external gate resistance.

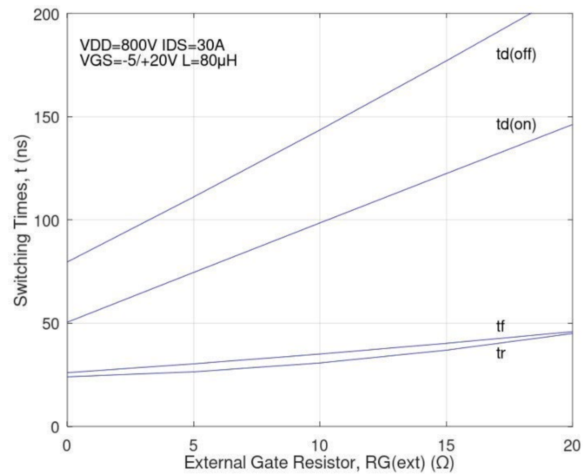

Figure 24: Clamped inductive switching energy vs. temperature.

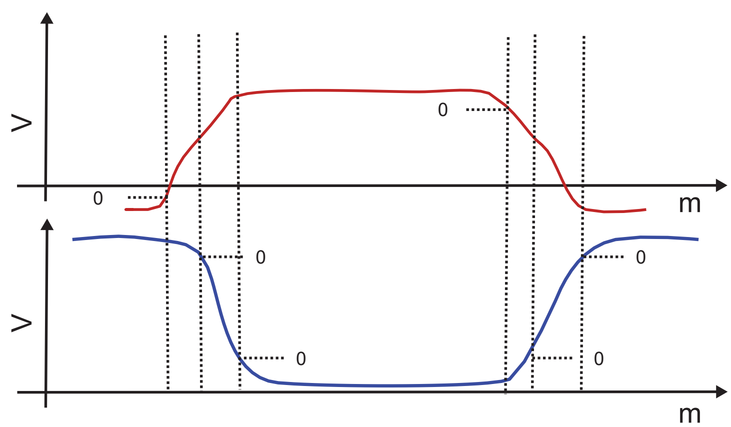

Figure 25: Timing references

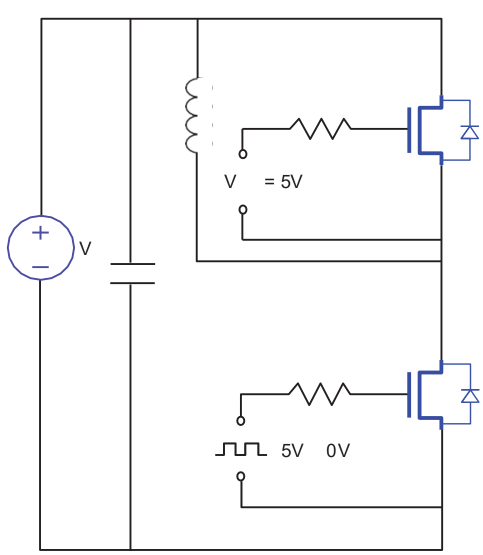

Figure 26: Clamped inductive switching waveform test circuit.

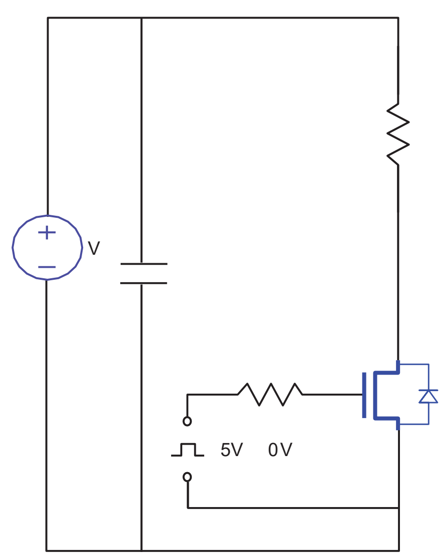

Figure 27: Gate charge test circuit.

Unless stated otherwise, temperature corresponds to junction temperature.

CAUTION: These devices are ESD sensitive. User proper handling procedures.

Disclaimer: The specifications provided are not a guarantee of component performance. It is essential to test components for their specific applications, as modifications may be required. Use of Cactus Materials components in life support systems and devices necessitates prior written approval from Cactus Materials.